V6063

3U VPX Versal® ASoC FPGA Optical I/O Module

Benefits

Heterogeneous computing card combining hard ARM processor cores, large FPGA fabric, AI Engines, and high-bandwidth interfaces

Designed specifically for sensor interface, AI workloads, digital signal processing, video processing, application co-processing, and secure networking

HPEC focus, 3U VPX, VITA 47 compliance, SOSA aligned options

Versatile design supports electrical or optical interfaces, optical options for both backplane or front-panel I/O

Modular optics for flexibility in supporting 1-25Gbs per lane

Features

Xilinx® Versal® ASoC (FPGA): VM1502/VM1802/VC1902

Up to twelve (12) 1G to 25G optical ports via MPO front panel I/O or VITA 66 optical backplane I/O

2 banks of 4GB up to 1866MHz LPDDR4 SDRAM

PCIe Gen3/Gen4 support

Thermal sensors for monitoring card temperature

Robust FPGA development framework

Overview

The V6063 is a next generation heterogeneous embedded computing 3U VPX module featuring the Xilinx® Versal® Adaptive System-on-Chip (ASoC), rugged optical and electrical high-speed IO, and SOSA aligned profile options. The V6063 provides options for Versal® Prime or Versal® AI Core part selection. In a single 3U VPX card, the V6063 provides three 100G optical interfaces (300Gbps aggregate), large FPGA fabric, ARM processor cores, and optional AI engines.

The V6063 excels at high-bandwidth interface applications where data is processed or pre-processed locally and then distributed across the VPX backplane or optical interfaces. Use cases include sensor interface, data processing, data distribution, and FPGA co-processing applications. Radar, signals intelligence, electronic warfare, video, storage, medical imaging, and embedded communications systems all can benefit from the V6063 module.

By leveraging the Versal® hard silicon Ethernet interfaces, PCIe controllers, DMA engines, and associated software drivers Xilinx® has enabled a robust ecosystem for high-bandwidth Ethernet performance. In addition to the Ethernet interfaces described, the FPGA fabric provided within the ASoC part is capable of hosting New Wave DV IP cores for Fibre Channel, ARINC-818, sFPDP, Aurora, and others. This makes the V6063 an ideal hardware platform for mixed interface protocol needs or protocol bridging applications.

The V6063 serves as a standalone data interface and processing solution in a single 3U VPX module. The V6063 provides twelve (12) full duplex optical ports supporting from 1-25Gb/s per lane, FPGA fabric resources, ARM processor cores, and AI/ML hard cores. The V6063 can also be used adjacent to CPUs and/or GPUs in a 3U VPX system. In this arrangement, the adjacent CPUs/GPUs are unburdened of the data interface overhead and can be dedicated to running high value applications and algorithms with the V6063 feeding them data directly across the backplane.

XILINX VERSAL™

SOSA™ Sensor Open Systems Architecture MEMBER

FIREFLY™

V6063

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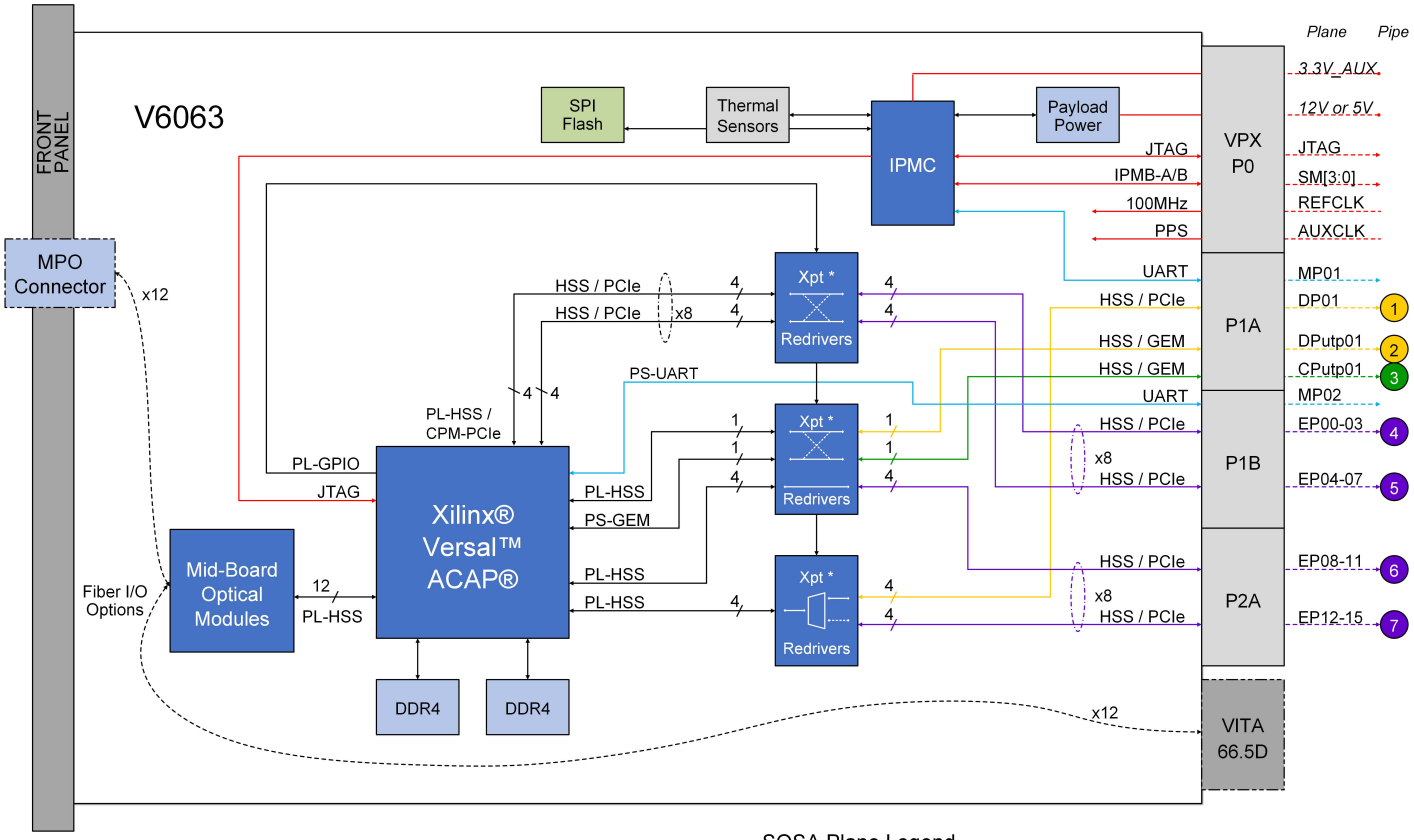


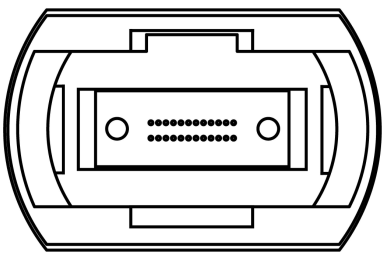
> V6063 Block Diagram

Optical Connector Options

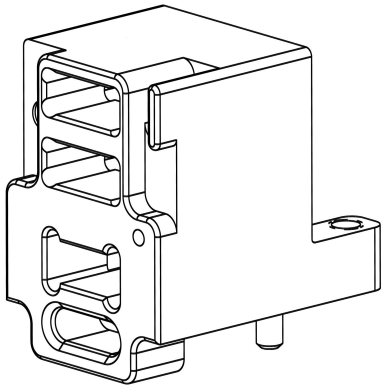
The V6063 offers three different optical I/O options:

1. **Optical Front Panel MPO Connector**
2. **Optical Backplane MT Connector for VITA 66.5**
3. **No optics**

1. Front Panel MPO (Female) I/O



2. VITA 66.5 Backplane MT I/O[1]



[1]Termination: VITA 66.5 Style D (pictured)

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Multi-Processor Multi-Core Support

The V6063 is uniquely suited for system architectures involving multiple processing cards on a common switched data plane. Specifically, the V6063 supports shared access from multiple host processors, enabling it to function as a cost-effective, high-performance gateway. This feature enables a single high-speed pipe to carry multiple virtual channels in systems that need to spread or load-balance sensor data across processor arrays.

Complete Product Support Program

New Wave DV prides itself on its excellent customer support, a fact that is echoed by our customers. New Wave DV provides industry standard warranty on its products, but it is the human factor that makes our support so valuable to our customers. Our team takes the time and effort to ensure that the customer experience with our products is a positive one.

Our Commitment

New Wave DV is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Our products, complete with the Development Framework, are intended to offer our customers an entirely unique out-of-the-box experience.

Technical Specifications

NETWORK INTERFACE
Up to twelve (12) 1G to 25G optical ports (front & backplane options)
• 850nm multi-mode optics
16 lanes of electrical high-speed network IO available to the backplane

OPTIONAL ADDITONAL PROTOCOLS
Ethernet, Fibre Channel, sFPDP, ARINC 818, Aurora

ASoC (FPGA) DEVICE
Xilinx® Versal® VM1502, VM1802, VC1902
Visit Xilinx® Versal® Datasheet[3]

MEMORY
2 banks of 4GB up to 1866MHz LPDDR4 SDRAM

PCIe INTERFACE
Two PCI Express Gen4/Gen3 x8 Interfaces
Four PCI Express Gen4/Gen3 x4 Interfaces

THERMAL SENSORS
2 digital temperature sensors

COMPLIANCE
VITA 47, 66.5

PHYSICAL CHARACTERISTICS
Dimensions:
170.75mm length: Face of carrier to back edge of Guide pin connectors
189.22mm length: MPO flip door to back edge of Guide pin connectors
100mm width: Edge of guide rail to guide rail
24.64mm height: From primary cover to secondary cover

Weight:
<1.764 lbs (800g)

POWER CHARACTERISTICS
Power Draw: 75W
Power Supply: 12V. 5V available by request.

TEMPERATURE
Operating: -40˚ C to 85˚ C (conduction-cooled)
Storage: -55˚ C to 105˚ C

[1]Xilinx® Versal® ASoC Datasheet: https://www.xilinx.com/products/silicon-devices/acap/versal.html

V6063 Hardware Part Number Configuration

Optional

400	-	06063	-	"WXYZ"	-	"IP"	-	"CC"
Series		Model		Board Configuration		IP Configuration		Coating Configuration
				Select 1 for each W, X, Y, and Z		Select 1 IP Option		Select 1 Coating Option

400-06063-[W][X][Y][Z]-[IP]-[CC]

W

Config #	Description
4+	*Reserved*
3	Xilinx Versal VC1902 ACAP
2	*Reserved*
1	Xilinx Versal VM1802 ACAP
0	Xilinx Versal VM1502 ACAP

Y

Config #	Description
0	Conduction cooled, 1" pitch

Z

Config #	Description
1+	*Reserved*
0	Industrial Temp

IP

Config #	Description
1+	Reserved
00	Example design package

CC

Config #	Description
AR	Acrylic conformal coat
UR	Urethane conformal coat
ER	Epoxy conformal coat
SR	Silicone conformal coat
XY	Parylene conformal coat
BLANK	No conformal coat

X

Config #	Slot Profile Description	VITA 65 Compatible Profile	VITA 65 Aperture Style
I+	*Reserved*	*n/a*	*n/a*
H	No optics populated, P2A not populated	14.6.11-0	J*
G	12-lane 1-10Gbps front panel MPO optics, P2A not populated	14.6.11-0	J*
F	12-lane 1-25Gbps front panel MPO optics, P2A not populated	14.6.11-0	J*
E	12-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated	14.6.11-14	J*
D	12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated	14.6.11-14	J*
C	8-lane 1-10Gbps front panel MPO optics, P2A not populated	14.6.11-0	J*
B	8-lane 1-25Gbps front panel MPO optics, P2A not populated	14.6.11-0	J*
A	8-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated	14.6.11-14	J*
9	8-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated	14.6.11-14	J*
8	No optics populated, P2A populated	14.6.13-0	J
7	12-lane 1-10Gbps front panel MPO optics, P2A populated	14.6.13-0	J
6	12-lane 1-25Gbps front panel MPO optics, P2A populated	14.6.13-0	J
5	12-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J
4	12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J
3	8-lane 1-10Gbps front panel MPO optics, P2A populated	14.6.13-0	J
2	8-lane 1-25Gbps front panel MPO optics, P2A populated	14.6.13-0	J
1	8-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J
0	8-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated	14.6.13-8	J

*14.6.11 Specifies an H style aperture with 2 style C fiber connectors, or an alternative style connector(s) that fit with the aperture space. 14.6.11 options 9, A, D, and E and 14.6.13 options 0, 1, 4 and 5 are delivered with a single style D connector thus meeting the specification of Style H or Style J.

V6063 “Go-Fast” Hardware Part Numbers

Part Numbers from Table 2 are available with the shortest lead times.

Table 2

Config #	Slot Profile Description
“.11” Profiles	
400-06063-1D00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-1E00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, 12-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-1H00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, optics not populated, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-3D00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-3E00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, 12-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-3H00-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, optics not populated, P2A not populated, conduction cooled, 1” pitch, industrial temp, example design package

“.13” Profiles	
400-06063-1400-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-1500-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, 12-lane 1-10Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-1800-00	V6063 FPGA 3U VPX Module, Xilinx Versal VM1802 ACAP, optics not populated, P2A populated, conduction cooled, 1” pitch, Industrial temp, example design package
400-06063-3400-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, 12-lane 1-25 Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-3500-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, 12-lane 1-10 Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package
400-06063-3800-00	V6063 FPGA 3U VPX Module, Xilinx Versal VC1902 ACAP, optics not populated, P2A populated, conduction cooled, 1” pitch, industrial temp, example design package

FOR MORE INFORMATION
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