

Supporting Legacy & High-Speed Protocols with the SOSA™ Technical Standard using COTS XMCs

*The Open Group FACE™ and SOSA™ US Air Force
TIM Paper by:*

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Executive Summary

Most aircraft in use by the U.S. Military use legacy protocols not supported within the SOSA™ Technical Standard. Additionally, there are high-speed protocols not currently available on “standard” COTS I/O Intensive and Compute Intensive SBCs, such as 100GbE, requiring support. This white paper will highlight how the use of COTS XMCs can support both legacy and leading-edge networks and actually “go faster” while implementing the SOSA Technical Standard.

Using XMCs within the SOSA Technical Standard

The SOSA Technical Standard was developed to provide an open system reference architecture for sensor systems. This architecture provides the benefits of a Modular Open Systems Approach (MOSA) and is aiming to bring sensor systems to the Warfighter in a more rapid and cost-effective way by addressing some of the known impediments inherent in the DoD acquisition process. As stated in the SOSA Technical Standard, “The SOSA Consortium strives to develop an ecosystem that allows interoperability, reuse, and faster delivery of products to market through vertical integration from cables, mechanical interfaces, hardware, software, and system designs.” To facilitate this approach, the SOSA Technical Standard provides a prescribed definition of Plug-In Cards (PICs) and their module profiles to ensure that integrators have multiple sources for PICs to allow for standardization that supports re-use across systems and prevents vendor lock.

To achieve the goals and benefits from the SOSA™ Reference Architecture, it needs to be adopted as widely as possible. This means in addition to brand new platforms, upgrades to existing platforms are needed. The problem is many legacy platforms have interfaces and protocols that are not part of the SOSA Technical Standard. To “go fast” and provide a cost-effective solution, SOSA sensors need the ability to interface with legacy system interfaces as upgrading an entire platform network may not be an option.

Leveraging XMCs to access system-specific interfaces

The SOSA Technical Standard provides a means to support system-specific interfaces via mezzanine cards. Mezzanine cards, and more specifically, XMCs, are addressed in Section 13.2.7 of the SOSA Technical Standard. The 3U I/O Intensive SBC provides an XMC site and a mapping of the XMC pins on Pn6 to the backplane using ANSI/VITA 46.9 P1w9-X12d, X8d, and X16s. The 3U I/O-Intensive SBC Slot Profile SLT3-PAY1F1F2U1T1U1T-14.2.16 is shown in Figure 1. In addition to the XMC mapping on Pn6, there is usually a PCIe interface connecting the XMC to the host processor on the SBC over Pn5. The SOSA Technical Standard also provides several XMC overlays for security functions and GPIO/GPLVDS in addition to the user-defined mapping. Under the SOSA Technical Standard, mezzanines are qualified while installed on the target Payload Module (Observation 13.2.7-1).

Support of Legacy & High-Speed Protocols with the SOSA™ Technical Standard using XMCs

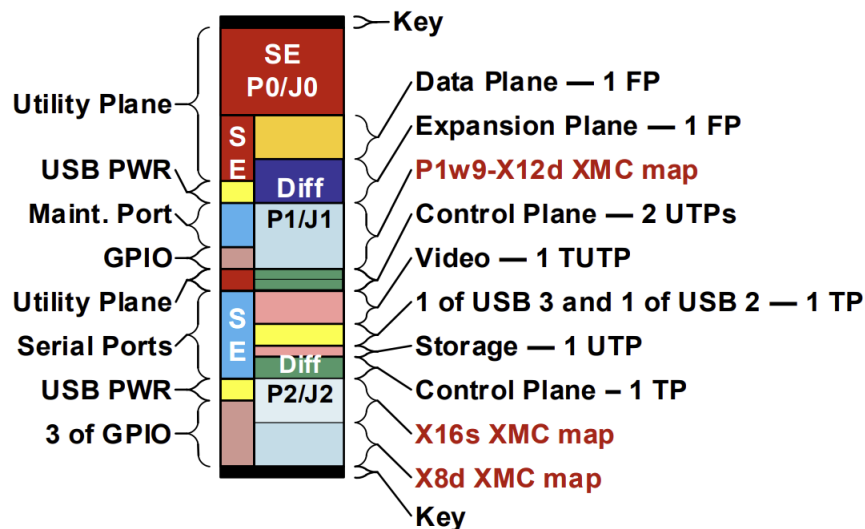


Figure 1: ANSI/VITA 65.0 3U I/O-Intensive SBC Slot Profile SLT3-PAY1F1F2U1TU1T1U1T-14.2.16

DoD platforms are active for extended periods of time and will go through several upgrades over their service lives to take advantage of emerging technologies, especially in the rapidly changing electronics industry. One of the items not always updated is the original network designed into a platform because of the expense of changing out the cable plant. This means when the platform does receive an electronics upgrade, the new equipment may need to interoperate with the legacy network and systems that were not selected for upgrade. This provides an issue for the Systems Integrators who may need to connect modern SOSA sensors to legacy system interfaces. Looking at a few real-world examples, the F/A-18E/F, EA-18G, F-15 and F-35 all use various Fibre Channel (FC) protocols. The F-22 has several proprietary high-speed 8B/10B interfaces, and many platforms use ANSI/VITA 17.1 sFPDP for radar systems.

Upgrading every legacy sensor and network interface on a platform becomes exorbitant in cost, but there is great benefit in enabling legacy platforms with SOSA sensor systems. The simplest and most cost-effective approach to interoperability with system-specific interfaces is leveraging COTS XMCs. This is not only the path recommended by the SOSA Technical Standard but has the benefit of localizing the system-specific interfaces to the XMC. This eliminates the need for board modifications to the I/O Intensive SBC and allows for upgrades in the future, with continuing support for legacy interfaces via the XMC.

Example application

To demonstrate the XMC approach and highlight its flexibility, the following scenario is offered. A sensor on the F/A-18 Super Hornet that is connected to the FC network needs to be upgraded, but the platform FC network must remain. To maximize the use of COTS hardware, a COTS XMC with FPGA is used to provide the FC interface on the platform. The Sensor Processing system consists of 1 – I/O Intensive SBC, 3 – Payload PICs and a Power Supply as outlined in Figure 2. The XMC is integrated with the I/O Intensive SBC to provide the legacy FC interface. There is a PCIe interface over Pn5 from the processor on the SBC to the FPGA on the XMC and the high-speed serial transceivers on the FPGA are mapped to the backplane via Pn6 using ANSI/VITA 46.9. This effectively provides an FC adapter to the I/O Intensive SBC to isolate the system-specific FC interface. The use of a XMC to address the legacy network interfaces allows the System Integrator to implement a new SOSA sensor that maintains connection with the legacy platform.

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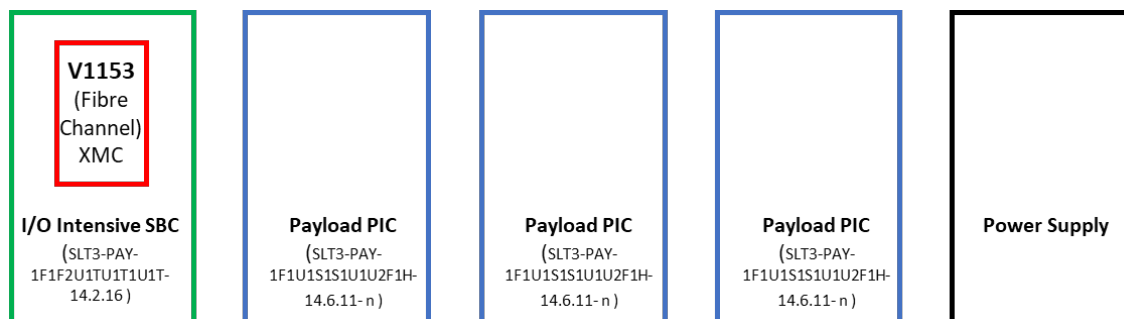


Figure 2: Example system with I/O Intensive SBC and XMC providing FC Interface

New Wave DV provides several FPGA-based XMCs along with numerous high-speed serial protocol IPs enabling a variety of protocol adapters for an I/O Intensive SBC. The V1153 is one example and the high-level block diagram for this card is provided in Figure 3. As you can see in the diagram, up to 8 high-speed serial transceivers from the FPGA are routed to the backplane via the ANSI/VITA 46.9 mapping on the I/O Intensive SBC. A PCIe-Gen 3 (x8) interface is provided over Pn5 to the SBC. In this specific case, the FPGA would be loaded with FC-specific IP providing an FC adapter to the SBC. The FC network would be isolated from the rest of the SOSA sensor.

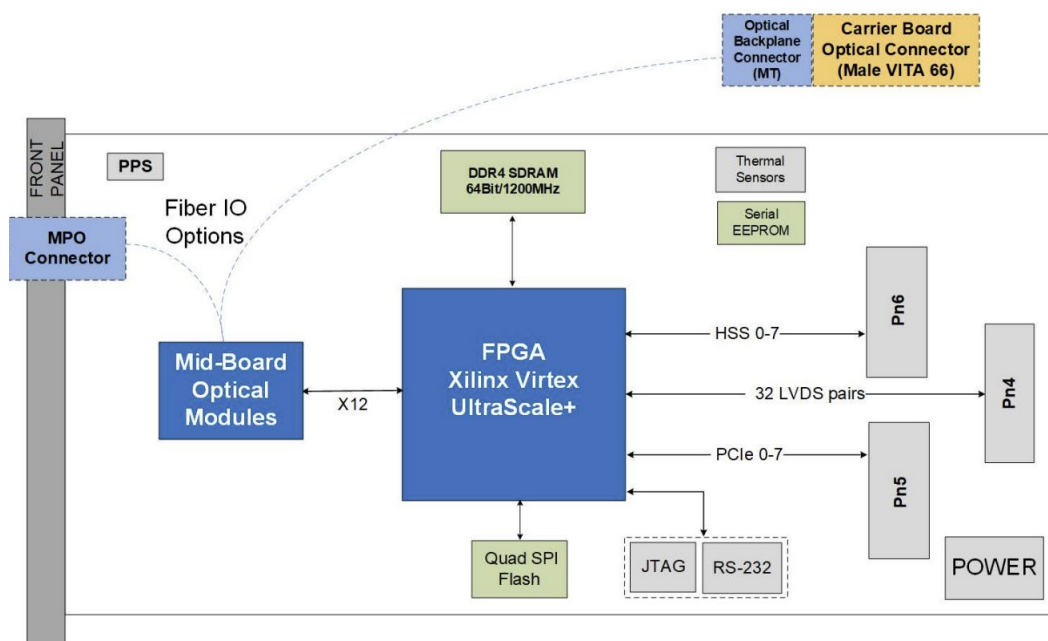


Figure 3: New Wave DV V1153 with Xilinx US/US+ FPGA

Because the various protocols are implemented in programmable logic in the FPGA, the same hardware configuration can support a variety of protocols with a simple FPGA image update. This allows the same hardware system to support platforms with different system-specific interfaces. Going back to the FC example above, the same system could be utilized in the Eurofighter platform where sFPDP is used as shown in Figure 4. All PICs from the FC system could be used in the new system by simply changing the IP on the

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FPGA XMC from FC to sFPDP. This highlights how a SOSA sensor has the flexibility to interoperate with multiple platform-specific interfaces that are not part of the SOSA Technical Standard. The SOSA sensor could be used on various platforms and connect to each platform's system-specific interface. COTS I/O Intensive SBCs can support multiple platforms without special modifications for each platform eliminating the need for costly, time-consuming NRE.

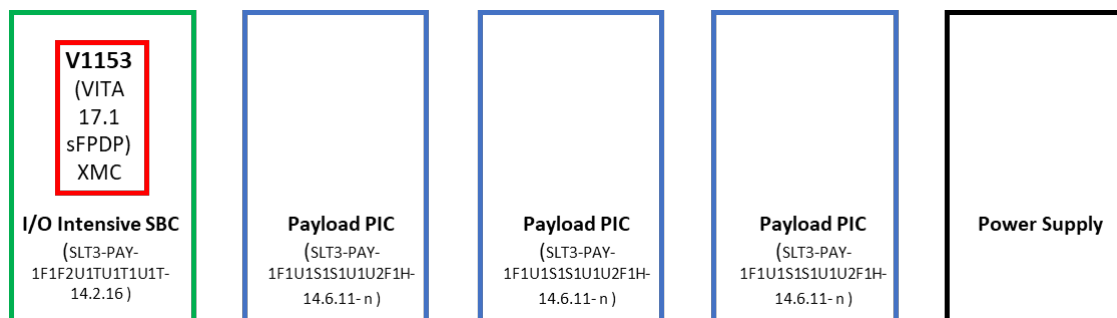


Figure 4: Example system with I/O Intensive SBC and XMC providing sFPDP Interface

Leveraging XMCs to create SOSA™ aligned PICs with increased capability

Another method of utilizing an XMC to “move fast” while adopting recent technologies within the SOSA Technical Standard is to rapidly create a new SOSA PIC with enhanced network functionality by integrating an XMC with an already existing SOSA PIC. This can be especially useful for providing an emerging interface or offload capability the original PIC does not support without having to spin a new card.

There are XMCs available with mid-board optical interfaces terminating with an MT connector compatible with the ANSI/VITA 66.5 standard utilized by some SOSA PICs. New Wave DV XMCs provide this capability with Samtec FireFly™ optical modules and can support up to 3 fat pipes on a single XMC. These XMCs have been successfully integrated with several 3U VPX modules to date. The result is a new 3U VPX module with a high-speed optical interface to the backplane.

Figure 5 and Figure 6 below are examples of New Wave DV XMCs that can provide an optical Ethernet interface to a host module. Both cards feature an NVIDIA® Mellanox® ConnectX®-5 Ethernet adapter chip capable of up to 2 ports of 100G Ethernet and many protocol offloads including UDP, TCP, RoCEv2, and others. In either case, up to a PCIe-Gen 4 (x8) interface is provided over Pn5 to the host processor. The V1161 adds a Xilinx® Versal® ACAP in conjunction with the ConnectX®-5, putting even more options like co-processing, data filtering, and decimation at the fingertips of system integrators.

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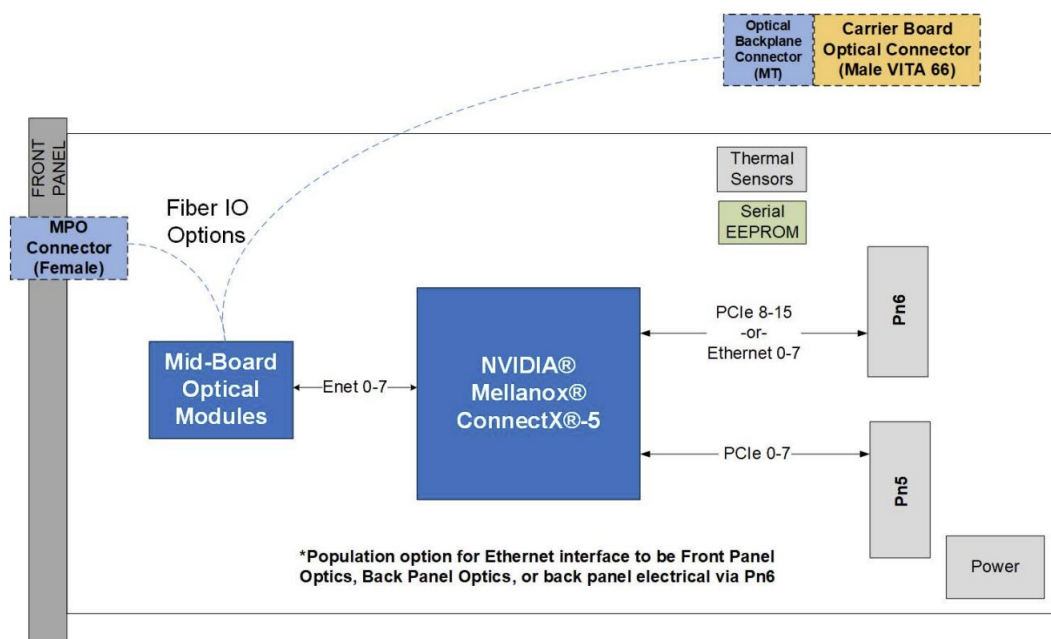


Figure 5: New Wave DV V1160 with NVIDIA® Mellanox® ConnectX®-5

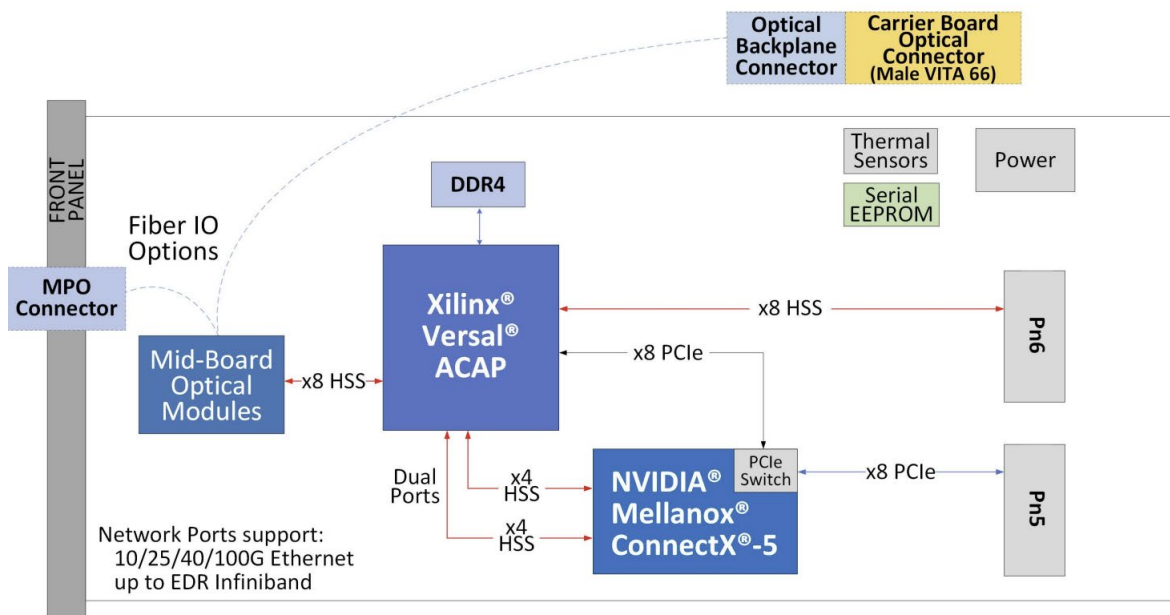


Figure 6: New Wave DV V1161 with Xilinx® Versal® ACAP and NVIDIA® Mellanox® ConnectX®-5

Revisiting the example system from Figure 4 with 1 – I/O Intensive SBC, 3 – Payload PICs and a Power Supply, one could imagine a system requirement for bringing optical 40G or 100G Ethernet to one of the Payload PICs. This could be an issue if none of the Payload PICs support the interface natively and many

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Compute Intensive SBCs currently available do not. One option for rapidly adding this capability would be to utilize an existing XMC with 40G or 100G Ethernet support.

Assume a Payload PIC follows the ANSI/VITA 65.0 Payload Slot Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11- n slot profile shown in Figure 7. By providing an insert in VITA 65 Aperture H that supports an MT, this Payload PIC can be quickly transformed into a new Payload PIC with an ANSI/VITA 66.5 optical interface. The new Payload PIC could be run through the SOSA Conformance Program to verify the new interface, and now the integrator has a new Payload PIC with an NVIDIA® Mellanox® ConnectX®-5 100G Ethernet interface without the cost of doing a major PCB redesign.

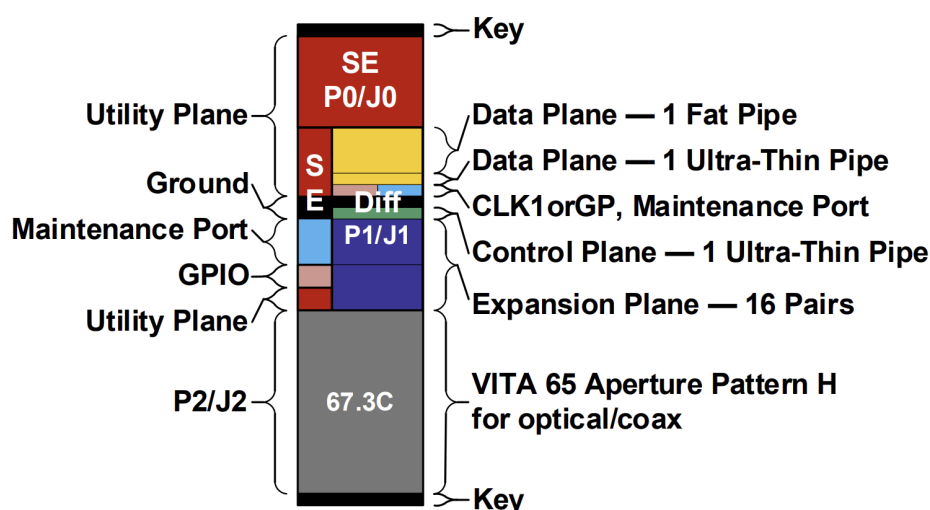


Figure 7: ANSI/VITA 65.0 Payload Slot Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11- n

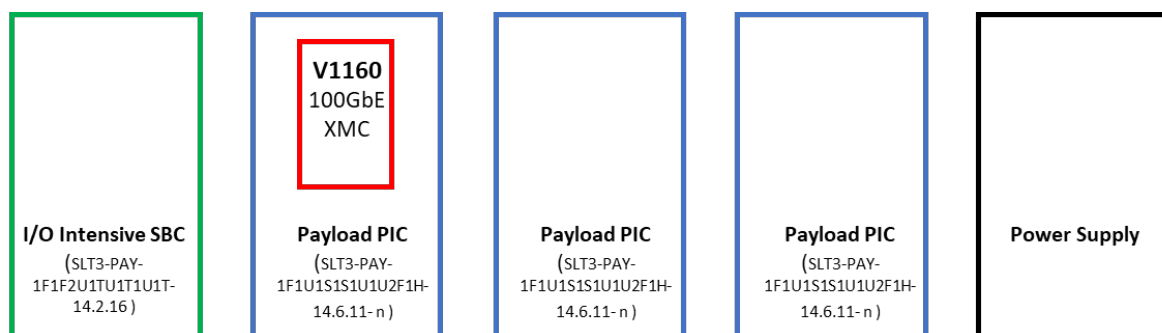


Figure 8: Example system with Payload PIC that has rapidly enabled 100G Ethernet capability

This example can be extended further by adding an XMC with an FPGA. Now, any Payload PIC with an XMC site (including a Compute Intensive SBC) can rapidly add support for any of the optical protocols supported by the SOSA Technical Standard including 40G/100G Ethernet, Aurora, and PCIe. Additionally, protocol offloads, data manipulation, decimation, filtering, and co-processing can also be done, all in one single slot.

Summary

Modern COTS XMCs enable integrators to create, support, and upgrade an existing platform's unique networking requirements in a clean, isolated way that aligns with the SOSA Technical Standard. They also allow a system designer to quickly create new SOSA PICs with increased functionality in a single slot. Leveraging COTS XMCs in alignment with the SOSA Technical Standard as demonstrated in this paper can expand the addressable market for SOSA sensor systems and will provide the DoD and its allies a more responsive and cost-effective supply chain. The use of XMCs to address network requirements not readily available from COTS suppliers will provide the DoD the ability to upgrade their systems rapidly and economically while achieving MOSA objectives.

References

(Please note that the links below are good at the time of writing but cannot be guaranteed for the future.)

- Technical Standard for SOSA™ Reference Architecture, Edition 1.0 (C212), published by The Open Group, September 2021; refer to: www.opengroup.org/library/c212
- ANSI/VITA 46.9-2018: VPX: PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard; refer to: www.vita.com/Standards
- VITA 66.5: VPX: Optical Interconnect on VPX – Hybrid Variant; refer to: www.vita.com/Standards
- ANSI/VITA 65.0-2021: OpenVPX™ System Standard; refer to: www.vita.com/Standards
- ANSI/VITA 17.1-2015: Serial Front Panel Data Port; refer to: www.vita.com/Standards

About the Author(s)

Ryan Jansen, Chief Architect

Ryan joined New Wave DV in 2012 and is currently in charge of Research & Development and New Product Direction. He has a deep knowledge of New Wave DV products and over 15 years of experience in the Mil-Aero/Defense industry. His primary focus has been embedded computing including FPGAs, high-speed networking, and board design. Ryan received his M.S. in Electrical Engineering from Columbia University and his B.S. in Electrical Engineering from the University of St. Thomas in St. Paul, MN.

Mark Grovak, Director, Strategic Business Development

Mark joined New Wave DV after a 40-year career in the Military Avionics market. He has led successful pursuits in providing avionics to the majority of aircraft in the DoD inventory starting with the F-14D through the F-35. Mark received his BA in Managerial Accounting and MBA in Government Contracts from the University of St. Thomas in St. Paul, MN. He is also a retired Navy Supply Corps officer.

About The Open Group FACE™ Consortium

The Open Group Future Airborne Capability Environment™ Consortium (the FACE™ Consortium), was formed as a government and industry partnership to define an open avionics environment for all military airborne platform types. Today, it is an aviation-focused professional group made up of industry suppliers, customers, academia, and users. The FACE Consortium provides a vendor-neutral forum for industry and government to work together to develop and consolidate the open standards, best practices, guidance documents, and business strategy necessary for acquisition of affordable software systems that promote innovation and rapid integration of portable capabilities across global defense programs.

Further information on the FACE Consortium is available at www.opengroup.org/face.

About The Open Group SOSA™ Consortium

The Open Group SOSA™ Consortium enables government and industry to collaboratively develop open standards and best practices to enable, enhance, and accelerate the deployment of affordable, capable, interoperable sensor systems. The SOSA Consortium is creating open system reference architectures applicable to military and commercial sensor systems and a business model that balances stakeholder interests. The architectures employ modular design and use widely supported, consensus-based, nonproprietary standards for key interfaces.

Further information on the SOSA Consortium is available at www.opengroup.org/sosa.

About The Open Group

The Open Group is a global consortium that enables the achievement of business objectives through technology standards. With more than 870 member organizations, we have a diverse membership that spans all sectors of the technology community – customers, systems and solutions suppliers, tool vendors, integrators and consultants, as well as academics and researchers.

The mission of The Open Group is to drive the creation of Boundaryless Information Flow™ achieved by:

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- Working with suppliers, consortia, and standards bodies to develop consensus and facilitate interoperability, to evolve and integrate specifications and open source technologies
- Offering a comprehensive set of services to enhance the operational efficiency of consortia
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