PRODUCT PREVIEW

Test Solution for Serial RapidIO® Protocol*

PXIe Test Instrument for Serial RapidIO® Protocol

Applications

Functional test and performance characterization of sRIO® equipment

Emulation/simulation of sRIO® equipment and systems

Benefits

Flexible test configuration with software/LabVIEW control of test instrument

Complete FPGA design with FPGA-based offload of protocol. No FPGA design needed by user

Reduce development time by focusing on software test applications instead of test hardware development

Lower total cost of test development and test system operation

Specifications

6 mini-SAS HD (SFF-8644) 1x4 ports

- Copper or active optical cables supported
- 1, 2, or 4 lane sRIO per port
- 1.25, 2.5, 3.125, 5 Gbaud per lane
- Port output disable via the PXI Trigger Bus

sRIO® Revision 2.1, Parts 1, 2, 3, 6, 7, 9, 10

Fully-compatible and programmable with LabVIEW

Up to 256 byte data payload

8-bit and 16-bit DevID

34-bit and 50-bit addressing

Packet support:

- Type 2 (NREAD non-atomic)
- Type 5 (NWRITE, NWRITE_R non-atomic)
- Type 6 (SWRITE)
- Type 8 (Maintenance)
- Type 9 (Data Streaming)
- Type 10 (Doorbell)
- Type 11 (Data Message)

National Instruments PXIe-7902 card

Overview

The sRIO® Test Instruments integrates up to four independent sRIO® interfaces into the LabVIEW environment using the National Instruments PXIe-7902 card. The FPGA core is designed and optimized for test and verification applications in a variety of conditions and is available with Labview support or Windows C API. Non-performance critical sRIO® functions are implemented in software for maximum flexibility and development ease, but performance critical functions are off-loaded to FPGA hardware.

The Test Instrument can be operated in two modes: an interface mode and a scripted test mode. In interface mode, the user can control the sRIO® interfaces in real time via software. Test mode is conducted via scripted operations where the user specifies all facets of the transaction including header info, payload, packet type, and cadence/timing of operations before handing off execution to the hardware. During both modes, all incoming and outgoing packets are time stamped, recorded and logged for user review. Both modes of functionality can also be further integrated into LabVIEW TestStand.

*This product is still currently in development with tentative release date in Q3 of 2020. New Wave DV is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Sign up for our News Wave newsletter to stay up-to-date with this and other product releases from New Wave DV. Visit newwavedv.com to view our other high-speed serial solutions.

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Contact New Wave DV today for more information.
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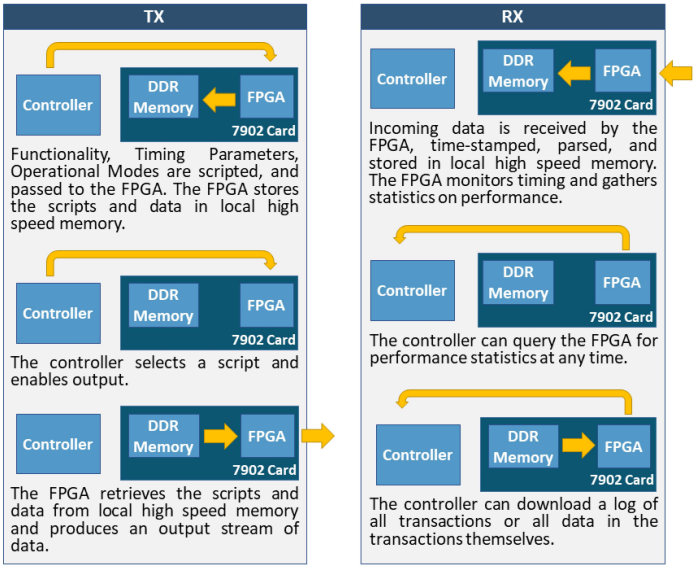

> sRIO® Test and Validation System Architecture

Our Commitment

New Wave DV is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Our products, complete with the Development Framework, are intended to offer our customers an entirely unique out-of-the-box experience.

Complete Product Support Program

New Wave DV prides itself on its excellent customer support, a fact that is echoed by our customers. New Wave DV provides industry standard warranty on its products, but it is the human factor that makes our support so valuable to our customers. Our team takes the time and effort to ensure that the customer experience with our products is a positive one.

Features

Fully-programmable sRIO® traffic patterns

Hardware offload of performance critical traffic flows

- Script engine defines transaction mix, hardware executes script at wire speed.
- Hardware transmit and receive logs with time-stamping

DRAM transmit and receive packet buffers

DMA channels from DRAM to host

Record all transactions with hardware time-stamping

Error detection and injection

User-definable packets

Configurable as host or device

Windows C or LabVIEW API and example designs

Configuration

PXIe HARDWARE:
PXIe-7902 NI PXI High-Speed Serial Instrument

NETWORK INTERFACE:
Up to 16 TX/RX lanes over 4 ports

PROTOCOL:
Serial RapidIO®

Ordering Information

400-784232-01-XX: NI PXIe-7902R High-speed Serial Instrument, Serial RapidIO® IP Core

Contact New Wave DV today **for more information.**

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